

# MAXIM

## 5Gbps PC Board Equalizer

MAX3784

### General Description

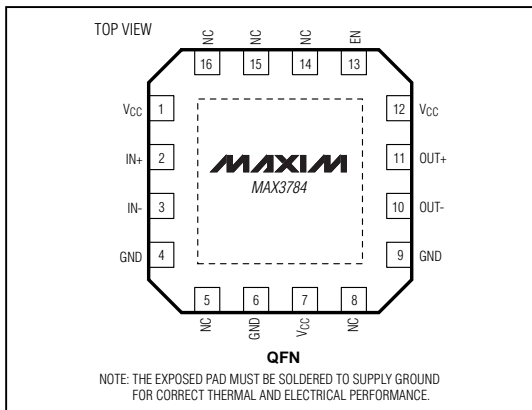
The MAX3784 5Gbps equalizer provides compensation for transmission-medium losses in up to 40in of FR4. It is optimized for short run length, balanced codes such as 8b10b, as found in multiplexed 1.25Gbps Ethernet systems.

The equalizer uses differential CML data inputs and outputs. A standby mode provides low power when the part is not in use. The MAX3784 is available in a 4mm × 4mm 16-pin QFN package that consumes only 185mW at +3.3V.

### Features

- ✦ Spans 40in (1m) of FR4 PC Board
- ✦ 0.18UI Deterministic Jitter up to 40in
- ✦ Low Power 185mW
- ✦ Equalization Reduces Intersymbol Interference
- ✦ Single +3.3V Supply
- ✦ Standby Mode
- ✦ Small 4mm × 4mm 16-Pin QFN Package

### Pin Configuration



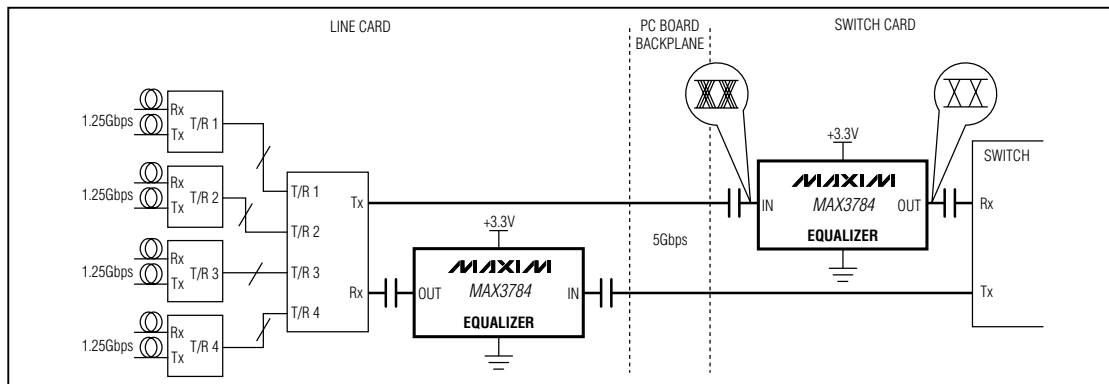
### Applications

Chassis Life Extension

### Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3784UGE	0°C to +85°C	16 QFN

### Typical Application Circuit



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## ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V<sub>CC</sub> .....-0.5V to +6V  
 Input Voltage .....(-0.5V) to (V<sub>CC</sub> + 0.5)V  
 Continuous Output Current .....-25mA to +25mA  
 Continuous Power Dissipation (T<sub>A</sub> = +85°C)  
 16-Pin QFN (derate 25mW/°C above +85°C) .. 1600mW

Operating Ambient Temperature Range .....0°C to +85°C  
 Storage Temperature Range .....-55°C to +150°C  
 Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +3V to +3.6V, T<sub>A</sub> = 0°C to +85°C. Typical values are at V<sub>CC</sub> = +3.3V and T<sub>A</sub> = +25°C unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Power		EN = low			30	mW
		EN = high		185	250	
Supply Noise Tolerance		(Note 8)	10Hz < f < 100Hz	100		mV <sub>P-P</sub>
			100Hz < f < 1MHz	40		
			1MHz < f < 2.5GHz	10		
Latency		From input to output		200		ps
<b>CML RECEIVER INPUT</b>						
Input Voltage Swing	V <sub>IN</sub>	Measured differentially at point A in Figure 1 (Note 4)	400		1000	mV <sub>P-P</sub>
Return Loss		100MHz to 2.5GHz		15		dB
Input Resistance		Differential	80	100	120	Ω
<b>EQUALIZATION</b>						
Residual Deterministic Jitter, 5Gbps		Table 1 (Notes 2, 3, 4, 7)	20in	0.13	0.21	UI <sub>P-P</sub>
			40in	0.18	0.23	
Residual Deterministic Jitter, 2.5Gbps		Table 1 (Notes 2, 3, 4, 7)	20in	0.08	0.14	UI <sub>P-P</sub>
			40in	0.13	0.28	
Residual Deterministic Jitter, 1.25Gbps		Table 1 (Notes 2, 3, 4, 7)	20in	0.04	0.07	UI <sub>P-P</sub>
			40in	0.07	0.15	
Random Jitter		(Notes 6, 7)		1.3	1.9	psRMS
<b>CML TRANSMITTER OUTPUT</b> (into 100Ω ±1Ω)						
Output Voltage Swing	V <sub>O</sub>	Differential swing, measured differentially at point C in Figure 1	400		600	mV <sub>P-P</sub>
Transition Time	t <sub>f</sub> , t <sub>r</sub>	20% to 80% (Notes 1, 7)	30	45	60	ps
Output Resistance		Single-ended	40	50	60	Ω

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## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>CC</sub> = +3V to +3.6V, T<sub>A</sub> = 0°C to +85°C. Typical values are at V<sub>CC</sub> = +3.3V and T<sub>A</sub> = +25°C unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>ENABLE CONTROL PIN</b>						
Input High Voltage			1.5			V
Input Low Voltage					0.5	V
Input High Current		(Note 5)	-150		10	μA
Input Low Current		(Note 5)	-150		10	μA

**Note 1:** Using 00 0001 1111 or equivalent pattern. Measured over entire input voltage range, max and min media loss and within 2in of output pins.

**Note 2:** Difference in deterministic jitter between reference points A and C in figure 1.

**Note 3:** Signal source amplitude range is 400mV<sub>p-p</sub> to 1000mV<sub>p-p</sub>, differential. Signal is applied differentially at point A as shown in Figure 1. The deterministic jitter at point B must be from media-induced loss and not from clock-source modulation. Deterministic jitter is measured at the 50% vertical level of the signal at point C.

**Note 4:** Test pattern. This is a combination of K28.5± characters running at the full bit rate and at one-quarter the bit rate. This simulates the multiplexing of four each 1.25Gbps Ethernet data streams.

Pattern (hex) 100 bits

00 FFFF F0F0 FF 0000 0F0F (quarter rate K28.5+, quarter rate K28.5-)  
3EB05 (K28.5± 00 1111 1010 11 0000 0101)

**Note 5:** On-chip pullup resistor of 40kΩ typical. Negative current indicates equalizer sources current.

**Note 6:** Test pattern is K28.5 with 40in trace.

**Note 7:** Guaranteed by design and characterization.

**Note 8:** Allowed supply noise during jitter tests.